



H15C/4/14/04  
N.E. *et al.*  
PATENT  
260/085

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

**Bulent Dervisoglu, et al.**

**Serial No.: 09/765,958**

**Filed:** January 18, 2001

**For:** HIERARCHICAL TEST CIRCUIT  
STRUCTURE FOR CHIPS WITH  
MULTIPLE CIRCUIT BLOCKS

Group Art Unit: 2133

Examiner: Dooley, Matthew C.

OK TO enter  
4/23/04  
M. D.

RECEIVED

APR 13 2004

Technology Center 2100

MAIL STOP AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AFTER FINAL RESPONSE PURSUANT TO 37 CFR § 1.116**

Sir:

With regard to the Final Office Action mailed February 17, 2004, please take the following action and consider the remarks below.

Please enter the accompanying Terminal Disclaimer.

A Terminal Disclaimer under 37 C.F.R 1.321(c) is submitted herewith to overcome the obvious-type double patenting rejection of the pending claims 1, and 15-23.

**Amendments to the claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks** begin on page 4 of this paper.